

1. For the same given specifications the order of the Butterworth filter N_b when compared with the order of the Chebyshev filter N_c

a.

b.

c.

d.

2. The frequency response of the Chebyshev type - 1 filter for even ordered filter starts at

a. 1

b. N

c.

d.

3. The magnitude response of the following filter decreases monotonically as frequency increases

a. Butterworth Filter

b. Chebyshev type - 1

c. Chebyshev type - 2

d. FIR Filter

4. The transition band is more in

a. Butterworth Filter

b. Chebyshev type - 1

c. Chebyshev type - 2

d. FIR Filter

5. The poles of Butterworth filter lies on

a. sphere

b. circle

c. ellipse

d. parabola

6. IIR digital filters are of the following nature

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a. Recursive

b. Non Recursive

c. Reversible

d. Non Reversible

7. In IIR digital filter the present output depends on

a. Present and previous Inputs only

b. Present input and previous outputs only

c. Present input only

d. Present Input, Previous input and output

8. Which of the following is best suited for IIR filter when compared with the FIR filter

a. Lower sidelobes in stopband

b. Higher Sidelobes in stopband

c. Lower sidelobes in Passband

d. No sidelobes in stopband

9. In the case of IIR filter which of the following is true if the phase distortion is tolerable

a. More parameters for design

b. More memory requirement

c. Lower computational Complexity

d. Higher computational complexity

10. A causal and stable IIR filter has

a. Linear phase

b. No Linear phase

c. Linear amplitude

d. No Amplitude

11. Neither the Impulse response nor the phase response of the analog filter is Preserved in the digital filter in the following method

a. The method of mapping of differentials

b. Impulse invariant method

c. Bilinear transformation

d. Matched Z - transformation technique

12. Out of the given IIR filters the following filter is the efficient one

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a. Circular filter

b. Elliptical filter

c. Rectangular filter

d. Chebyshev filter

13. What is the disadvantage of impulse invariant method

a. Aliasing

b. one to one mapping

c. anti aliasing

d. warping

14. Which of the I I R Filter design method is antialiasing method?

a. The method of mapping of differentials

b. Impulse invariant method

c. Bilinear transformation

d. Matched Z - transformation technique

15. The nonlinear relation between the analog and digital frequencies is called

a. aliasing

b. warping

c. prewarping

d. antialiasing

16. The most common technique for the design of I I R Digital filter is

a. Direct Method

b. In direct method

c. Recursive method

d. non recursive method

17. In the design a IIR Digital filter for the conversion of analog filter in to Digital domain the desirable property is

a. The axis in the s - plane should map outside the unit circle in the z - Plane

b. The Left Half Plane(LHP) of the s - plane should map in to the unit circle in the Z - Plane

c. The Left Half Plane(LHP) of the s-plane should map outside the unit circle in the z-Plane

d. The Right Half Plane(RHP) of the s-plane should map in to the unit circle in the Z - Plane

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18. In the IIR filter Design method by approximation of derivatives as Ω varies from to ∞ , the corresponding locus of a point in the z-plane is a circle with radius and center

- a. 0,0
- b. 1,1
- c. 1, - 1
- d.

19. In the Impulse Invariant method the ratio of

- a.
- b.
- c.
- d.

20. The I I R filter design method that overcomes the limitation of applicability to only Lowpass filter and a limited class of bandpass filters is

- a. Approximation of derivatives
- b. Impulse Invariance**
- c. Bilinear Transformation
- d. Frequency sampling

21. In the Frequency Transformations of the analog domain the transformation is

- a. Low Pass to Lowpass
- b. Lowpass to Highpass**
- c. Lowpass to Bandpass
- d. Lowpass to Bandreject

22. In the Frequency Transformations of the analog domain the transformation is

- a. Low Pass to Lowpass
- b. Lowpass to Highpass
- c. Lowpass to Bandpass
- d. Lowpass to Bandreject**

23. Frequency Transformations in the Analog domain and in the Digital domain will yield

- a. Same Results
- b. Different Results

c. Different results for Bilinear Transformation

d. Different Results except Bilinear Transformation

24. In the Frequency Transformations of the analog domain the transformation is

a. Low Pass to Lowpass

b. Lowpass to Highpass

c. Lowpass to Bandpass

d. Lowpass to Bandreject

25. In the Frequency Transformations of the analog domain the transformation is

a. Low Pass to Lowpass

b. Lowpass to Highpass

c. Lowpass to Bandpass

d. Lowpass to Bandreject

26. In the Impulse Invariance method the mapping from analog frequency Ω to the digital frequency ω is

a. one to one

b. one to many

c. many to many

d. many to one

27. In the Frequency transformations in the digital domain involves mapping z with

a. $g(z)$

b. $g(z)$

c. $1/g(z)$

d. $1/g(z)$

28. A discrete impulse function is applied to the inputs of four different filters. The output sequences of these filters are listed below. Which one of these filters has a pole outside the unit circle?

a. $\{1, 2, 3, 4, 5, 6, 0, 0, 0, \dots\}$

b. $\{1, -1, 1, -1, 1, -1, \dots\}$

c. $\{1, 2, 4, 8, 16, \dots\}$

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d. $\{1, 0.5, 0.25, 0.125, \dots\}$

29. A discrete impulse function is applied to the inputs of four different filters. For each of the output sequences that follow, state whether the filter is nonrecursive.

a. $\{1, 2, 3, 4, 5, 6, 0, 0, 0, \dots\}$

b. $\{1, -1, 1, -1, 1, -1, \dots\}$

c. $\{1, 2, 4, 8, 16, \dots\}$

d. $\{1, 0.5, 0.25, 0.125, \dots\}$

30. A filter has the difference equation: $y(nT) = x(nT) + x(nT - T)$. What traditional filter type best describes this filter?

a. Integrator

b. differentiator

c. subtractor

d. multiplier

31. The FIR filters will have constant group delay and not phase delay when the impulse response is antisymmetrical about

a.

b.

c.

d.

32. The Linear Phase symmetric Impulse response having even number of samples cannot be used to design the following filter

a. Lowpass

b. Highpass

c. Bandpass

d. Bandstop

33. The phase response of FIR filters with linear phase is given by

a.

b.

c.

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d.

34. In a Linear Phase FIR Filters the phase delay and group delay are related as

a.

b.

c.

d.

35. The FIR filters will have constant phase delay and group delays when the impulse response is symmetrical about

a.

b.

c.

d.

36. The following filter is always stable

a. Butterworth filter

b. Chebyshev filter

c. IIR filter

d. FIR filter

37. Which of the filter can be realized in both recursive and non recursive structure?

a. Butterworth filter

b. Chebyshev filter

c. IIR filter

d. FIR filter

38. Which filter is free of Limit cycle oscillations when implemented on a finite word length digital system

a. Butterworth filter

b. Chebyshev filter

c. IIR filter

d. FIR filter

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39. The transfer function of FIR Causal filter is given by

a.

b.

c.

d.

40. In which filter the memory requirement and execution time are very high

a. Butterworth filter

b. Chebyshev filter

c. IIR filter

d. FIR filter

41. Which of the following window is used instead of Hanning window for the same main lobe width

a. Rectangular window

b. Triangular window

c. Hamming window

d. Kaiser Window

42. The cascaded form of realization is used

a. When complex poles with absolute magnitude less than one

b. When complex poles with absolute magnitude greater than one

c. When complex zeros with absolute magnitude less than one

d. When complex zeros with absolute magnitude greater than one

43. In the following window the amplitude of the sidelobes is unaffected by the length of the window

a. Rectangular window

b. Triangular window

c. Hamming window

d. Kaiser window

44. In which of the following windows the transition region is more and stopband attenuation is less

a. Rectangular window

b. Triangular window

c. Hamming window

d. Kaiser window

45. The mainlobe width of the Hanning window is twice that of

a. Rectangular window

b. Triangular window

c. Hamming window

d. Kaiser window

46. To obtain FIR Filter, from the infinite Fourier series the series is truncated at

a.

b.

c.

d.

47. The Gibbs oscillations are due to

a. Abrupt truncation of the Fourier series

b. No truncation of the Fourier series

c. Abrupt termination of the Fourier transform

d. Slow termination of the Fourier series

48. One of the desirable characteristic of the window is that the central lobe of the frequency response of the window should contain

a. Most of the energy and should be narrow

b. Lowest energy and should be narrow

c. Most of the energy and should be broad

d. Lowest of the energy and should be broad

49. In a window the desirable characteristic is that the sidelobes of the frequency response should

a. Increase in energy rapidly as ω tends to π

b. Decrease in energy rapidly as ω tends to π

c. Increase in frequency response

d. Contain most of the energy and should be narrow

50. Which window has the advantage of flexibility of sidelobe level and N ?

- a. Rectangular window
- b. Triangular window
- c. Hamming window
- d. Kaiser window**

51. In which filter closed form design equations exist

- a. FIR Filter
- b. I I R Filter**
- c. Butterworth
- d. Chebyshev

52. In which filter all the poles are located at origin

- a. FIR Filter**
- b. I I R Filter
- c. Butterworth
- d. Chebyshev

53. In which filter high selectivity can be achieved by using higher order

- a. FIR Filter**
- b. I I R Filter
- c. Butterworth
- d. Chebyshev

54. Which filter has less flexibility specially for obtaining non-standard frequency response

- a. FIR Filter
- b. I I R Filter**
- c. Butterworth
- d. Chebyshev

55. Which filter design methods are iterative procedures that require powerful Computational facilities for Implementation

- a. FIR Filter**
- b. I I R Filter
- c. Butterworth
- d. Chebyshev

56. Frequency sampling method is suitable for

a. Broad band frequency selective filters

b. Narrow band frequency selective filters

c. Passband frequency selective filters

d. Stopband frequency selective filters

57. The frequency sample method can be improved by

a. Introducing the stopband

b. Introducing ripples

c. Introducing the transition samples

d. Eliminating the transition samples

58. In the frequency sampling method the Peak sidelobe level can be reduced by

a. Increasing Transition width

b. Decreasing Transition width

c. Increasing Ripples

d. Decreasing Ripples

59. In which of the following filter the errors due to round off noise are more

a. FIR Filter

b. IIR Filter

c. Butterworth

d. Chebyshev

60. In which of the following filter the poles are placed anywhere inside the Unit circle and not always stable is

a. FIR Filter

b. IIR Filter

c. Butterworth

d. Chebyshev

61. When the input rate F_x is greater than the output rate F_y in the sampling rate Conversion the Lowpass filter acts as

a. anti - aliasing prefilter

b. anti - imaging postfilter

c. anti - aliasing postfilter

d. anti - imaging prefilter

62. When the input rate F_x is greater than the output rate F_y in the sampling rate Conversion the Lowpass filter removes the spectral replicas at multiples of

- a. F_x
- b. $I F_x$
- c. F_y**
- d. $I F_y$

63. An Increase in the sampling rate by an integer factor I can be accomplished by interpolating

- a. $I - 1$ samples between successive values**
- b. $I - 1$ samples between alternate values
- c. $I - 2$ samples between successive values
- d. $I - 2$ samples between alternate values

64. For the sampling rate conversion process by a factor of the processes are

- a. First Interpolation and then decimation**
- b. First Decimation and then Interpolation
- c. First Extrapolation and then Decimation
- d. First Decimation and then Extrapolation

65. In the Sampling rate conversion both the up sampling filter and down sampling filters can be replaced with a single

- a. Highpass filter
- b. Bandpass filter
- c. Lowpass filter**
- d. Bandstop

66. Sampling rate conversion by any rational factor can be obtained with

- a. only decimation
- b. only interpolation
- c. only extrapolation
- d. decimation and Interpolation**

67. The Process of sampling rate conversion is

- a. Only Resampling

b. Only Reconstruction

c. Resampling after Reconstruction

d. Reconstruction after Resampling

68. In the decimation process, the down sampling operation in combination with filtering on a linear time invariant system results in

a. linear time invariant

b. Linear time variant

c. Non Linear time invariant

d. Nonlinear time - invariant

69. The Implementation of sampling rate conversion requires the use of the following Filter

a. Linear time - invariant filter

b. Linear time - variant filter

c. Non Linear time - Invariant filter

d. Non Linear time - variant filter

70. In the Down sampling process the frequency range of the input signal

a. stretches by a factor D

b. compresses by a factor D

c. stretches by a factor $2D$

d. compresses by a factor $2D$

71. Which of the following is not an application of multirate Digital signal processing?

a. Digital filter banks

b. Subband coding

c. Broadband filters

d. Transmultiplexers

72. The CIC filter structure is

a. Combinational Impulse Cascade

b. Cascade Integrator Comb

c. Cascade Impulse Comb

d. Combinational Integrated Impulse

73. For the development of Polyphase decimator which of the following is used

a. Commutator

- b. Decommutator
- c. Communicator
- d. Transmitter

74. For the efficient software Implementation of Rational sampling rate conversion the following filter is used

- a. I I R filter
- b. FIR filter**
- c. Butterworth filter
- d. Chebyshev filter

75. When the output rate F_y is greater than the output rate F_x in the sampling rate Conversion the Lowpass filter removes the spectral replicas at multiples of

- a. F_x**
- b. $1 F_x$
- c. F_y
- d. $1 F_y$

76. When the output rate F_y is greater than the output rate F_x in the sampling rate Conversion the Lowpass filter acts as

- a. anti - aliasing prefilter
- b. anti - imaging postfilter**
- c. anti - aliasing postfilter
- d. anti - imaging prefilter

77. Polyphase filter Structures are used for

- a. Up sampling
- b. Down sampling
- c. Sampling Rate Conversion**
- d. anti - aliasing

78. The Polyphase filter structures are suitable for

- a. FIR Filters
- b. I I R Filter
- c. FIR and I I R filters**
- d. analog filter

79. The order of the sampling rate converter and a linear time - invariant system can be interchanged by changing

- a. Upsampling rate
- b. Down sampling rate
- c. Filter system function**
- d. Input function

80. Von Neumann architecture consists of

- a. one address bus and one data bus**
- b. two address buses and two data buses
- c. only data bus and no address bus
- d. only address bus and no data bus

81. Harvard Architecture consists of

- a. one address bus and one data bus
- b. two address buses and two data buses**
- c. only data bus and no address bus
- d. only address bus and no data bus

82. Which of the following processor uses the Zero - Overhead loop buffer feature?

- a. Microprocessor
- b. Microcontroller
- c. DSP Processor**
- d. Nanoprocessor

83. The DSP processor for high efficiency uses

- a. Low memory Bandwidth
- b. High memory Bandwidth**
- c. Low Bandwidth
- d. High Bandwidth

84. Which addressing mode allows processor to access data sequentially and then automatically wrap around to the beginning address

- a. Direct addressing mode
- b. Indirect addressing mode
- c. Circular addressing mode**

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d. Register Addressing mode

85. Which of the processor is the fast among the following

a. Microprocessor

b. Microcontroller

c. DSP Processor

d. Nanoprocessor

86. The feature in which the DSP Processor is superior to advanced microprocessor is

a. High Cost

b. High Power

c. High Computational Speed

d. Real time I/O capability

87. The number of memory accesses per clock per period that can be achieved using on chip DARAM of a DSP is

a. 1

b. 2

c. 3

d. 4

88. Which of the following architecture is used in the DSP processor?

a. Von Neumann architecture

b. Harvard Architecture

c. Traditional Microprocessor architecture

d. Traditional Microcontroller architecture

89. Which of the following processors does not contain Timer?

a. Microprocessor

b. Microcontroller

c. DSP Processor

d. Nanoprocessor

90. After the Execution of the Instruction MACD pgm,dma the content of dma is copied to

a. dma

b. dma +1

c. dma - 1

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d. dma +2

91. What is SIMD Architecture

a. Single Instruction, Multiple Data

b. Simulation Instruction, Multiple Data

c. Superscalar Instruction, Multiple Data

d. Similar Instruction, Multiple Data

92. The Texas Instrument 320C5X Processor consists of

a. Separate Multiplexer and Adder

b. Separate Multiplier and adder

c. Dedicated Multiplier Accumulator

d. Dedicated Medium Access Controller

93. For the MAC operation the output of a Multiplier is stored in

a. Adder

b. Accumulator

c. Product Register

d. ALU

94. In the TMS320C5X Processor the MACD Instruction corresponds to

a. Multiple Accumulators Delay

b. Multiplexed Accumulator Delay

c. Multiply Accumulate With Data shift

d. Medium Access Controller Delay

95. One of the most common operations required in digital signal processing applications is

a. Array addition

b. Array Subtraction

c. Array Multiplication

d. Array Division

96. The DSP Processor array Multiplication requires

a. Single Multiplier and adder

b. Single Multiplier

c. Single adder

d. Single Subtractor

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97. The following two four bit number multiplication 1011 and 1100 take how many Clock cycles in the DSP Processor Hardware

- a. One
- b. Two
- c. Three
- d. Four

98. In the DSP Processor MAC Corresponds to

- a. Multiple Accumulators
- b. Multiplexed Accumulator
- c. Multiplier Accumulator**
- d. Medium Access Controller

99. In the Motorola DSP Processor DSP5600X consists of

- a. Separate Multiplexer and Adder
- b. Separate Multiplier and adder
- c. Dedicated Multiplier Accumulator**
- d. Dedicated Medium Access Controller

100. The Purpose of multiported memory of the DSP Processor is

- a. Decreasing the number of accesses/clock period
- b. Increasing the number of accesses/clock period**
- c. Storing the Program and data in the same memory
- d. Decrease the Chip area

101. DARAM connected to a DSP with two independent data and address buses can be Used to achieve

- a. Two memory accesses/clock period**
- b. Three memory accesses/clock period
- c. Four memory accesses/clock period
- d. Six memory accesses/clock period

102. Processors with multiple memory banks provide usually a small amount of memory on - chip

- a. a small amount of on - chip memory**
- b. a large amount of on - chip memory

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- c. a large amount of off - chip memory
- d. no on - chip memory

103. The purpose of Program Cache of the DSP Processor is

- a. To eliminate to access the main memory for certain instructions**
- b. To enable access to the main memory for all instructions
- c. To enable access to the auxiliary memory for all instructions
- d. To eliminate access to the auxiliary memory for all instructions

104. DSP processors caches are in general only used for

- a. Program Instructions and data Instructions
- b. Program instructions and not for data Instructions**
- c. Data instructions and not for Program Instructions
- d. Address Instructions and not for Program Instructions

105. In which of the following architecture Processor is connected to two memories via independent buses

- a. Von Neumann Architecture
- b. Harvard Architecture

c. Modified Harvard Architecture

- d. Modified Von Neumann Architecture

106. Implementation of the FIR filter needs for the four memory accesses using Von Neumann architecture takes _____ Instruction cycles

- a. One
- b. Two
- c. Three

d. Four

107. Implementation of the FIR filter needs for the four memory accesses using Harvard Architecture takes _____ clock cycles

- a. One
- b. Two
- c. Three**
- d. Four

108. Implementation of the FIR filter needs for the four memory accesses using Advanced Harvard Architecture takes _____ clock cycles

- a. One
- b. Two**
- c. Three
- d. Four

109. DSP processors generally provide only _____ off - chip buses

- a. One
- b. Two**
- c. Three
- d. Four

110. The addressing mode that uses both read pointer and write pointer is

- a. Direct addressing mode
- b. Register addressing mode
- c. Bit reversed addressing Mode
- d. Circular addressing mode**

111. The pipeline operation

- a. Increases the number of clock cycles
- b. Increase the number of Instructions
- c. Increases the time

d. Decrease the number of clock cycles

112. The addressing mode that is much useful in computing the FFT

- a. Direct addressing mode
- b. Register addressing mode
- c. Bit reversed addressing Mode**
- d. Circular addressing mode

113. The addressing mode that is much useful in computing the FIR Filter and uses a Sliding window is

- a. Direct addressing mode
- b. Register addressing mode
- c. Bit reversed addressing Mode

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d. Circular addressing mode

114. Circular buffer of the circular addressing mode uses the following register

a. Block size register

b. Block address register

c. Block access register

d. Block Execution register

115. VLIW Approach is used by

a. SIMD Architecture

b. Multi Issue Architecture

c. Multi Bus Architecture

d. Multi Register Architecture

116. Which architecture Keeps the routing information within each sub - instruction

a. SIMD Architecture

b. VLIW Architecture

c. Multi Bus Architecture

d. Multi Register Architecture

117. SIMD architecture is only effective in algorithms that can process data

a. parallel

b. serially

c. continuously

d. discontinuously

118. Which of the following DSP Processor architecture can not be used in cellular Phones

a. SIMD Architecture

b. Multi Issue Architecture

c. Multi Bus Architecture

d. Multi Register Architecture

119. TMS320C6X DSP Processor is based on the following Architecture

a. SIMD

b. VLSIW

c. Superscalar

d. Userdefined

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120. The C3X Processor which is having on - chip ROM is

- a. C30
- b. C31
- c. C31
- d. C32

121. The Cache size of C3X Processor is

- a. 64K
- b. 64 words
- c. 4K
- d. 2K

122. Which bits present in the ST register of the C3X will globally disable and enable the interrupts

- a. GIE
- b. C
- c. Z
- d. OV

123. The Purpose of I/O flag register is

- a. to control the function of XF0 and XF1 pins
- b. to control the Interrupt operation
- c. to control the Read and Write operation
- d. to control the Program Memory

124. The number of registers used for the repeat instruction of C3X Processor are

- a. 2
- b. 3
- c. 4
- d. 1

125. The C3X Register file contains _____ Registers

- a. 12
- b. 24
- c. 28
- d. 34

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126. The number of data pages and location in each page of data memory of C3X Processor is

- a. 512,128K
- b. 256,64K**
- c. 256,32K
- d. 512,8K

127. The number of bits of DP used for direct addressing mode of C3X Processor are

- a. LSB 9 bits
- b. LSB 8 bits**
- c. LSB 12 bits
- d. all bits

128. The number of ARs used for indirect addressing mode of the C3X Processor are

- a. 2
- b. 3**
- c. 1
- d. 4

129. The number of flag bits present in the Status Register (ST) of C3X Processor are

- a. 4
- b. 6
- c. 9**
- d. 10

130. The host port is used for

- a. Serial communication
- b. Handshaking
- c. Control
- d. Interrupts**

131. The Comm ports are used for

- a. Internal communication
- b. Inter Processor Communication**
- c. Serial communication
- d. Parallel Communications

132. Which of the Following communication is faster

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a. Serial port

b. parallel port

c. TDM Port

d. Synchronous Port

133. The Parallel port Signal are generally used for

a. Serial communication

b. Handshaking

c. Control

d. Interrupts

134. The Bit I/O Ports are used for

a. Serial communication

b. Handshaking

c. Control

d. Interrupts

135. Which of the following is not the feature of a DSP Processor

a. Harvard Architecture

b. 2 - 4 memory accesses per cycle

c. caches on chip SRAM

d. Multiple bit shifts in one cycle

136. The Application of on - chip Timer is

a. Generation of non - periodic Interrupts and Sampling clocks for A/D Converter

b. Generation of periodic Interrupts and Sampling clocks for A/D Converter

c. Generation of periodic Interrupts and Sampling clocks for D/A Converter

d. Generation of Impulses and Filter coefficients

137. The serial port of the DSP Processor operates in

a. Only Asynchronous Mode

b. Synchronous mode only

c. Synchronous and asynchronous mode

d. Serial mode

138. The TDM port of the DSP Processor is

a. Parallel Port

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b. Serial Port

- c. Synchronous Port
- d. Asynchronous Port

139. The TDM port normally uses the following lines for serial communication

- a. one
- b. two
- c. three

d. four

140. The register in which the multiplicand is stored before multiplication is performed is _ _ _ _ _ and Is _ _ _ _ _ bit wide

- a. PREG, 32
- b. PREG, 16
- c. TREG0, 16
- d. TREG0, 32

141. _ _ _ _ _ permits the contents of memory to be left shifted by 0 - 16 bits before they are either Fed to ALU or stored from ALU to memory

- a. Scaling shifter
- b. ALU
- c. PLU

d. Auxiliary ALU

142. The _ _ _ _ _ permits execution of logical operations on data without affecting the contents of ACC.

a. Parallel logic unit

- b. Auxiliary ALU
- c. Central ALU
- d. Auxiliary Register Compare Register

143. The hardware multiplier unit in the C5X processors perform multiplication of _ _ _ _ _ times _ _ _ _ _ bit Represented in _ _ _ _ _ complement form.

- a. 16, 16, 1s
- b. 8, 8, 1s
- c. 16, 16, 2s

d. 8, 8, 2s

144. _____ Holds the result of multiplication and is _____ bit wide.

a. PREG, 32

b. PREG, 16

c. TREG0, 16

d. TREG0, 32

145. The 320C5X DSPs are said to have advanced Harvard architecture because

a. they have separate memory bus structures for program and data

b. they have instructions that enable data transfer between the program and data memory area

c. they have same memory bus structures for program and data

d. they contents of program memory cannot into the data memory or vice versa

146. The central ALU of C5X DSP processors have _____ bit ALU and one of the operands for the ALU operation comes from _____

a. 32, ACC

b. 16, ACC

c. 32, ACCB

d. 16, ACCB

147. The result of operations performed in central ALU are stored in _____

a. ACC

b. ACCB

c. TREG0

d. PREG

148. The ALU register whose either higher order word or lower order word can be loaded From memory is.

a. ACC

b. ACCB

c. TREG0

d. PREG

149. The _____ bit register used for temporary storage of accumulator is _____

a. 32, PREG

b. 32, ACCB

c. 16, TREG0

d. 32, ACC

150. The status register bit that determines whether multiplier's 32 - bit product is leftshifted by 0, 1, 4 or right shifted by 6 with sign extension before it is Transferred/added to the ACC is

a. PM

b. CNF

c. HM

d. XF

151. The RAM configuration control bit that indicates whether the on - chip Reconfigurable Dual access RAM is mapped to data space or program space is

a. PM

b. CNF

c. HM

d. XF

152. The bit of ST0 that determines whether the ACC is replaced with either largest positive or Negative number or left unmodified is -----

a. SXM

b. TC

c. OV

d. OVM

153. The bit of ST1 that is used for testing whether a particular memory is zero or not or for comparing one register against another register memory is -----

a. SXM

b. TC

c. OV

d. OVM

154. The bit of ST1 that becomes 1 if either addition generates a carry or subtraction results in Borrow is -----

a. SXM

b. TC

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c. OV

d. C

155. The register that specifies the number of bits by which the scaling shifter should shift either the incoming data to one of the CPU register or vice versa is _____ and is _____ bit wide.

a. TREG1, 4

b. TREG1, 5

c. TREG2, 5

d. TREG2, 4

156. When the incoming data to CPU is left shifted by the scaling shifter the LSBs are filled with _____

a. 0

b. 1

c. LSB before shifting

d. MSB

157. The bit of status register ST1, which determines whether the MSBs of the bits left shifted by the scaling shifter is Zero, are sign extended is _____

a. SXM

b. TC

c. OV

d. OVM

158. In the hardware stack of C5X processors _____ bit numbers can be stored

a. 16, 16

b. 16, 8

c. 8, 8

d. 8, 16

159. The bit of status register 0(ST0) that becomes 1 if overflow occurs from an ALU operation is _____

a. SXM

b. TC

c. OV

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d. OVM

160. The number of User Maskable Interrupts in C5X DSP is

a. 11

b. 12

c. 13

d. 14

161. Which of the following is commonly used in multiprocessor applications

a. HPI

b. BSP

c. TDM

d. DARAM

162. The Size of Dual Access RAM (DARAM) of the C5X DSP is

a. 256 - word X 16 - bit

b. 512 - word X 16 - bit

c. 1024 - word X 16 - bit

d. 1056 - word X 16 - bit

163. The Width of the Hardware Timer of C5X DSP Processor is

a. 8 - bit

b. 16 - bit

c. 32 - bit

d. 64 - bit

164. The Number of serial ports available for different functions in C5X is

a. 2

b. 3

c. 4

d. 5

165. The bit of status register that determines whether the processor halts the internal operation while acknowledging a hold or not is _____

a. PM

b. CNF

c. HM

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d. XF

166. The _____ bit of status register indicates the status of the general purpose output pin.

a. PM

b. CNF

c. HM

d. XF

167. The pointers that are contained in the status register 0 are _____

a. ARP, DP

b. ARB, IPTR

c. RDPTR, WRPTR

d. INTM

168. The pointers that are contained in the status register 1 are _____

a. ARP

b. DP

c. ARB

d. IMTM

169. If _____ bit is set to 0, all unmasked interrupts are enabled. Otherwise all the maskable Interrupts are disabled.

a. ARP

b. DP

c. ARB

d. INTM

170. The number of ARAU s in the C3X Processors are

a. 2

b. 3

c. 1

d. 4

171. The number of index registers in the C3X Processors are

a. 3

b. 1

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c. 2

d. 4

172. The number of address buses present in the C3X family processors are

a. 8

b. 7

c. 9

d. 4

173. The Multiplier in the C3X family Processors can perform _ _ _ _ _ multiplications

a. 16 - bit integer

b. 24 - bit integer

c. 32 - bit floating point

d. 24 - bit integer and 32 - bit floating point

174. The size of C3X Processor ALU is

a. 24 - bits

b. 16 - bits

c. 32 - bits

d. 40 - bits

175. The C3X family processors are _ _ _ _ _ bit floating - point processors

a. 8

b. 16

c. 24

d. 32

176. The `C3X family processors suitable for low power application is

a. `C30

b. C31

c. LC31

d. C32

177. The on - chip RAM available in the C3X family processors is

a. 2K

b. 4K

c. 8K

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d. 64K

178. The C3X family Processors are different in

a. Architecture

b. Memory Size

c. Speed of operation

d. Peripherals

179. The number of data buses present in the C3X family processors are

a. 8

b. 7

c. 9

d. 4

180. The number of DMA Controllers in C32 Processor are

a. 1

b. 2

c. 3

d. 4

181. The C3X Processors have

a. Only SARAM

b. Only DARAM

c. SARAM and DARAM

d. Only ROM

182. The Number of Registers which control the timer operation is

a. 2

b. 3

c. 4

d. 1

183. The size of C3X Processor timer is

a. 32

b. 16

c. 24

d. 40

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184. The number of control registers for each serial port of C3X Processor are

- a. 4
- b. 5
- c. 7
- d. 8**

185. The address buses of the C3X Processor are of _____ width

- a. 32 bits
- b. 24 bits**
- c. 16 bits
- d. 40 bits

186. The On - chip RAM memory address location of the C3X Processor is

- a. 808000h - 80FFFFh
- b. 809800h - 809FFFh**
- c. 800000h - 80FFFFh
- d. 809800h - 80FFFFh

187. The segment start address register of C3X Processor cache is of size

- a. 19 bits**
- b. 20 bits
- c. 24 bits
- d. 32 bits

188. The cache available in the C3X Processor is for

- a. Program Memory**
- b. Data Memory
- c. Program and Data Memory
- d. Cache Memory

189. The number of serial ports in C31 and C32 Processors are

- a. 1**
- b. 2
- c. 3
- d. 4

190. What is a DAG Unit in the DSP Processor

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- a. Data Access General Unit
- b. Data Access Generation Unit
- c. Data Address Generation Unit**
- d. Direct Access Generation Unit

191. What is the PMST Register?

- a. Programmable Mode Status Register**
- b. Processor Mode Status Register
- c. Processor Mode Sign Register
- d. Programmable Mode Sign Register

192. In the TMS30C5402 internal memory the RAM is accessed as

- a. One access per block per cycle**
- b. Two accesses per block per cycle
- c. Three accesses per block per cycle.
- d. Four accesses per block per cycle

193. The function of the Barrel shifter in the DSP Processor is

- a. Only one bit shift in one clock cycle
- b. Multiple bit shifts in one clock cycle**
- c. Multiple bit shifts in multiple clock cycles
- d. No bit shifts

194. The CSSU of a DSP Processor is

- a. Common Subtract and Store Unit
- b. Compare Subtract and Store Unit
- c. Compare, Select, and Store Unit**
- d. Common Select and Store Unit

195. The particular TMS 320C54X Processor consists of

- a. one Program bus**
- b. two Program buses
- c. three Program buses
- d. four Program buses

196. TMS 320C54X Processor consists of

- a. One Data Bus

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b. Two Data Buses

c. Three Data Buses

d. Four Data Buses

197. TMS 320C54X Processor consists of

a. One Address Bus

b. Two Address Buses

c. Three Address Buses

d. Four Address Buses

198. The accumulator of TMS320C54X Processor is of length

a. 16 bit

b. 32 bit

c. 40 bit

d. 64 bit

199. The Purpose of Guard bits of Accumulator of TMS320XX Processor is for

a. Carry and overflow

b. MSB

c. LSB

d. Unused

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